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(54) Analog-to-digital converter.

(57) An analog-to-digital converter includes a plurality of digital-to-analog converting circuits, a control circuit connected to the digital-to-analog converting circuits to control the condition of the respective digital-to-analog converting circuits, a comparator having a first input connected commonly to outputs of the digital-to-analog converting circuits and a second input connected to receive a reference voltage, and a successive approximation register connected to an output of the comparator and adapted to control the control circuit. The control circuit is adapted to generate control signals to the respective digital-to-analog converting circuits in one-to-one relation so that the output potentials of the digital-to-analog converting circuits are successively incremented one after one by a potential corresponding to one bit.

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ANALOG-TO-DIGITAL CONVERTER

Background of the Invention

Field of the Invention

The present invention relates to an analog-to-digital converter, and more specifically to a successive approximation type analog-to-digital converter which includes a plurality of local digital-to-analog converters of a given resolution and which can provide a resolution higher than the given resolution of the digital-to-analog converter.

Description of related art

At present, digital technique has been widely used in various fields. As a result, analog-to-digital converters (called "A/D converter" hereinafter) and a digital-to-analog converter (called "D/A converter" hereinafter) become very important as an interface between an analog signal and a digital signal.

Among different types of A/D converters, a successive approximation type A/D converter is known as one which can operate at an intermediate or high speed and can provide a digital signal composed of a relatively large number of bits.

Referring to Figure 1, there is shown a block diagram of a typical example of a conventional successive approximation type A/D converter. The shown A/D converter includes an analog signal input terminal 10 connected to a first input of a sample and hold circuit 12, which has a second input conected to an output of a local D/A converter 14. The sample and hold circuit 12 has a pair of outputs corresponding to the pair of inputs, these outputs being connected to a pair of inputs of a comparator 16, whose output is connected to a successive approximation register 18. This register 18 has parallel outputs connected to the local D/A converter 14. Further, a serial output of the register 18 is connected to a digital signal output terminal 20.

With this arrangement, the local D/A converter is so set to generate a voltage $F_{FS}/2$ corresponding to a half of the full scale voltage V_{FS} when it receives the parallel output of the register 18 composed of the most significant bit (MSB) of "1" and the other bits of "0". In this condition, the voltage of the analog signal held in the sample and hold circuit 12 is compared with the output voltage $V_{FS}/2$ of the local D/A converter by the comparator 16. The result of comparison is outputted to the successive approximation register 18, which changes its content, i.e., a digital data to be supplied to the local D/A converter 14. For example, when the input analog signal is larger than $V_{FS}/2$, the MSB of the register 18 is maintained at "1" as it is, and the second significant bit (2SB) is changed to "1" from "0". The other bits are maintained at "0". Accordingly, the output voltage of the D/A converter 14 is brought into $3V_{FS}/4$. On the other hand, when the input analog signal is smaller that $V_{FS}/2$, the MSB and 2SB of the register 18 are changed to "0" and "1", respectively, and the other bits are maintained at "0". In this case, the D/A converter 14 generates $V_{FS}/4$. Thus, the value of the MSB is determined, and then, the next comparison is made between the input analog signal and the reference voltage $V_{FS}/4$ or $3V_{FS}/4$ of the local D/A converter 14, so that the 2SB will be determined. Thus, similar operation will be repeated to successively determine each bit of the digital data until the least significant bit (LSB) is determined.

In the above mentioned successive approximation A/D converter, the local D/A converter is generally divided into two types, one of which includes a resistor string or ladder and the other of which includes a capacitor array.

At present, D/A converters, which have a resolution of 8 bits to 10 bits and which can be used as the local D/A converter 14 in the above mentioned conventional successive approximation A/D converter, can be manufactured in mass production manner with high reliability and stability in accordance with recent advanced integrated circuit technique. Therefore, A/D converters having a relatively small bit number can be manufactured with reliability.

However, components fabricated on an integrated circuit have a certain limit in uniformity of characteristics, and therefore, it is the present status that it is difficult to obtain a D/A converter having a higher resolution. For example, in order to obtain a D/A converter having a resolution of 12 bits to 16 bits, it is necessary to constitute a circuit with discrete parts such as resistors and capacitors of the accuracy matching with the required resolution. Otherwise, it is necessary to use a fine adjustment means such as a Laser trimming. In this case, however, the cost for forming required elements becomes very large, and also, elements having a sufficient reliability cannot be obtained.

As mentioned above, in the case that a D/A converter of a large bit number is constituted in combination with a single resistor string or ladder of a single capacitor array, a sufficient accuracy cannot be obtained because the D/A converter cannot maintain a monotonic increase over the full range because of dispersion of element characteristics. For overcoming this problem, there has been proposed to use a plurality of D/A converters in parallel. For example, if two D/A converters are combined in parallel, the combined D/A converter can have a full scale corresponding to the sum of respective full scales of the two unitary D/A converters. Assuming that first and second unitary D/A converters have full scales FS1 and FS2, respectively, the combined D/A converter has a full scale FS equal to (FS1 + FS2).

In the combined D/A converter, the first unitary D/A converter will increment its output in response to increment of a digital input. When the MSB of the digital input changes from "0" to "1", the logic value "1" is supplied to all input bits of the first unitary D/A converter so that it outputs its full scale FS1. Thereafter, the second unitary D/A converter will increment in response to increment of the digital input, so that the output of the second D/A converter is added to the output of the first D/A converter to provide a combined output.

Further, an interpolation type which uses a master D/A converter and a slave D/A converter has been proposed. In this case, one step of the master D/A converter is divided further finely by the slave D/A converter.

However, the first mentioned accumulation method using a plurality of unitary D/A converters in parallel is disadvantageous in that a gain error of each unitary D/A converter is accumulated, with the result that the overall D/A converter has a large error in total linearity. On the other hand, the interpolation type has such a defect that it cannot have a monotonic increase if a slave D/A converter has an increased step error.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an A/D converter which has overcome the above mentioned drawbacks of the conventional ones.

Another object of the present invention is to provide a successive approximation A/D converter which uses a plurality of D/A converters but which does not have a large gain error as a whole.

A further object of the present invention is to provide a successive approximation A/D converter which includes a plurality of D/A converters and has an improved linearity error.

The above and other objects of the present invention have been achieved in accordance with the present invention by an analog-to-digital converter which includes a plurality of digital-to-analog converting circuits, a control circuit connected to the digital-to-analog converting circuits to control the condition of the respective digital-to-analog converting circuits, a comparator having a first input connected commonly to outputs of the digital-to-analog converting circuits and a second input connected to receive a reference voltage, and a successive approximation register connected to an output of the comparator and adapted to control the control circuit, characterized in that the control circuit is adapted to generate control signals to the respective digital-to-analog converting circuits in one-to-one relation so that the output potentials of the digital-to-analog converting circuits are successively incremented one after one by a potential corresponding to one bit.

Preferably, each of the digital-to-analog converting circuit includes a charge redistribution binary weighted capacitor array. Specifically, each capacitor array is composed of a plurality of weighted capacitance capacitors which has not only charge redistribution function but also sample and hold function. Further, the second input of the comparator is connected to one terminal of a capacitor means whose other terminal is connected to the reference voltage, the capacitor means having a capicitance equal to the total capicitance of all the capacitors included in all of the digital-to-analog converting circuits.

The above other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram showing one example of the conventional successive approximation A/D converter;

Figure 2 is a block diagram showing a basic construction of the successive approximation A/D converter in accordance with the present invention;

Figure 3 is a more detailed block diagram of the A/D converter shown in Figure 2;

Figure 4 is a diagram illustrating a basic conception of the A/D converter shown in Figure 2;

Figure 5 is a diagram similar to Figure 3 but showing a first embodiment of the successive approximation A/D converter in accordance with the present invention;

Figure 6 is a circuit diagram of a switch control signal generator incorporated in the A/D converter shown in Figure 5;

Figure 7 is a diagram similar to Figure 3 but showing a second embodiment of the successive approximation A/D converter; and

Figure 8 is a diagram similar to Figure 6 but showing a switch control signal generator incorporated in the A/D converter shown in Figure 7.

Description of the Preferred Embodiments

Referring to Figure 2, there is shown a conceptual structure of the successive approximation A/D converter in accordance with the present invention. The shown A/D converter includes an analog signal input terminal 30 connected to an analog signal input circuit 32. This input circuit 32 has an output connected commonly to a plurality of local D/A converters 34A to 34K of the charge redistribution type which has a capacitor array functioning a charge redistribution and sample and hold capacitor for the first bit to the bit of 2^m. These local D/A converter has a resolution of "ℓ" bits. Outputs of all the D/A converters 34A to 34K are connected commonly to one input of the comparator 36.

This comparator 36 has another input connected to a capacitor 38, which is in turn connected to a reference potential terminal 40. The comparator 36 is connected at its output to a successive approximation register 42. This register 42 has parallel outputs connected to a generator 44 which supplies switch control signals to all the local D/A converters 34A to 34K so as to cause the respective D/A converters to change their internal condition. Further, the register 42 is adapted to output an digital signal of n bits. In this construction, the relation of $n = \ell + m$ and $K = 2^m$ is established.

With this arrangement, an analog signal is supplied from the input terminal 30 through the input circuit 32 to all the first to the k^{th} local D/A converters 34A to 34K. Specifically, the analog signal is sampled in the capacitor array of each D/A converters controlled by the control signal generator 44. Then, the analog signal input circuit 32 is cut off so that the analog signal is held in the respective capacitor array. Thereafter, comparison between the outputs of all the D/A converters and the reference potential is made by the comparator 36, and the content of the register 42 is modified on the basis of the comparison result. In response to the content of the register 42, the generator 44 generates such control signals to the D/A converters 34A to 34K that the condition of the capacitor arrays is successively modified one by one comparison. Thus, a digital signal of n bits is finally outputted from the register 42.

Turning to Figure 3, the register 42 has parallel bit outputs supplying n-bit data D_1, D_2, D_3 ... D_{n-1} and D_n to the generator 44. On the other hand, the first D/A converter 34A includes a capacitor array composed of $(\ell + 1)$ capacitors C_{10} to $C_{1\ell}$ which function as a charge redistribution and sample and hold capacitor. One electrodes of these capacitors C_{10} to $C_{1\ell}$ are connected to each other. The other electrode of each capacitor C_{10} to $C_{1\ell}$ is connected to a common terminal of a single pole triple throws switch S_{10} to $S_{1\ell}$. Each of the switches S_{10} to $S_{1\ell}$ has a first selection terminal connected to the analog signal input terminal 30, a second selection terminal connected to a first reference potential terminal 46, and a third selection terminal connected to a second reference potential terminal 48. Similarly, the second D/A converter 34B includes a capacitor array of $(\ell + 1)$ capacitors C_{20} to $C_{2\ell}$ and associated switches S_{20} to $S_{2\ell}$ connected as shown. Further, the other D/A converters each includes $(\ell + 1)$ capacitors and $(\ell + 1)$ associated switches. The commonly connected electrodes of the capacitors of each D/A converters 34A to 34K are also connected commonly to one input of the comparator 36.

The other input of the comparator 36 is connected through a capacitor 50 to a third reference potential terminal 40. The capacitor 50 is shunted by a switch 52, and the third reference potential terminal 40 is connected through another switch 34 to the one input of the comparator 36.

The above capacitors are in the following relation: The capacitor 50 has a capacitance C_c equal to the total capacitance of all capacitors $C_{10} \sim C_{1\ell}$, $C_{20} \sim C_{2\ell}$, ... $C_{k0} \sim C_{k\ell}$ included in all the D/A converters 34A to 34K. Further, assuming that a unitary capacitance is C, the capacitors $C_{10} \sim C_{1\ell}$, $C_{20} \sim C_{2\ell}$, ... , $C_{k0} \sim C_{k\ell}$ of each of the first to K^{th}D/A converters 34A to 34K are weighted to have capacitances C, C, 2C, ... , and $2^{(\ell-1)}$ C respectively. Therefore, $C_c = (K \times 2^{\ell})C$.

Before explaining the operation of the embodiment, description will be made on operation of a combined D/A converter which receive n bit data and which includes two (n-1) bit D/A converters, with references to Figure 4.

The n bit data DATA-A is divided into a portion of only LSB (the n^{th} bit) and a portion of $(n-1)^{th}$ bit to MSB. The latter portion is supplied as a (n-1) bit data DATA-B to one D/A converter DAC-2, and also inputted to a digital adder ADD-1. This adder adds the LSB of DATA-A to the LSB of DATA-B (i.e., the $(n-1)^{th}$ bit of DATA-A) and supplies the result of addition as another (n-1) bit data DATA-C to another D/A converter DAC-1. Outputs of the two D/A converters DAC-1 and DAC-2 are inputted to an analog adder ADD-2 which generates an analog signal corresponding to the input digital signal DATA-A.

Now, assuming n = 6, the digital data DATA-A, DATA-B and DATA-C are under the relation shown in the following TABLE-1.

TABLE 1

	"A" (6 Bits)	"B" (5 Bits)	"C" (5 Bits)
63	1 1 1 1 1 1	1 1 1 1 1	1 0 0 0 0 0
62	1 1 1 1 1 0	1 1 1 1 1	1 1 1 1 1
61	1 1 1 1 0 1	1 1 1 1 0	1 1 1 1 1
60	1 1 1 1 0 0	1 1 1 1 0	1 1 1 1 0
59	1 1 1 0 1 1	1 1 1 0 1	1 1 1 1 0
58	1 1 1 0 1 0	1 1 1 0 1	1 1 1 0 1
57	1 1 1 0 0 1	1 1 1 0 0	1 1 1 0 1
56	1 1 1 0 0 0	1 1 1 0 0	1 1 1 0 0
55	1 1 0 1 1 1	1 1 0 1 1	1 1 1 0 0
54	1 1 0 1 1 0	1 1 0 1 1	1 1 0 1 1
.	.	.	.
.	.	.	.
.	.	.	.
36	1 0 0 1 0 0	1 0 0 1 0	1 0 0 1 0
35	1 0 0 0 1 1	1 0 0 0 1	1 0 0 1 0
34	1 0 0 0 1 0	1 0 0 0 1	1 0 0 0 1
33	1 0 0 0 0 1	1 0 0 0 0	1 0 0 0 1
32	1 0 0 0 0 0	1 0 0 0 0	1 0 0 0 0
31	0 1 1 1 1 1	0 1 1 1 1	1 0 0 0 0
30	0 1 1 1 1 0	0 1 1 1 1	0 1 1 1 1
29	0 1 1 1 0 1	0 1 1 1 0	0 1 1 1 1
28	0 1 1 1 0 0	0 1 1 1 0	0 1 1 1 0
.	.	.	.
.	.	.	.
.	.	.	.
9	0 0 1 0 0 1	0 0 1 0 0	0 0 1 0 1
8	0 0 1 0 0 0	0 0 1 0 0	0 0 1 0 0
7	0 0 0 1 1 1	0 0 0 1 1	0 0 1 0 0
6	0 0 0 1 1 0	0 0 0 1 1	0 0 0 1 1
5	0 0 0 1 0 1	0 0 0 1 0	0 0 0 1 1
4	0 0 0 1 0 0	0 0 0 1 0	0 0 0 1 0
3	0 0 0 0 1 1	0 0 0 0 1	0 0 0 1 0
2	0 0 0 0 1 0	0 0 0 0 1	0 0 0 0 1
1	0 0 0 0 0 1	0 0 0 0 0	0 0 0 0 1
0	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0

As seen from the above TABLE-1, the (n-1) bit digital inputs to the D/A converters DAC-1 and DAC-2 are alternatively and successively incremented dependently upon the LSB of the input digital data.

Now, assume that the D/A converter DAC-1 has a gain of K, and the D/A converter DAC-2 has a gain of K-ΔK (where ΔK is a gain error between the DAC-1 and DAC-2). Further, assume n-1 = 1. Under this condition, the gain error appears at each increment of logic input, differently from the conventional accumulation manner using a plurality of D/A converters in parallel. However, the amount of error is

compressed to $1/2^{\ell}$. The reason for this is that the amount to be successively and alternatively incremented corresponds to the LSB of each D/A converter and therefore is equal to one step amount which can be obtained by dividing the full scale of the D/A converter output by 2^{ℓ}. Therefore, the gain error is also compressed at the same ratio.

Reviewing in detail, the outputs V_1 and V_2 of the DAC-1 and DAC-2 can be expressed as follows:

$$V_1 = K\left(\frac{1}{2}a_2 + \frac{1}{4}a_3 + \cdots + \frac{1}{2^{\ell}}\right)V_{REF}$$

$$V_2 = (K - \Delta K)\left(\frac{1}{2}a_2 + \frac{1}{4}a_3 + \cdots + \frac{1}{2^{\ell}}\right)V_{REF}$$

where V_{REF} is a reference potential supplied to DAC-1 and DAC-2.

Therefore, in the conventional accumulation method, the full scale output V_{FS} is

$V_{FS} = (2K - \Delta K)\, V_{REF}$

Thus, an ideal half scale output of the combined D/C converter is expressed:

$\frac{1}{2}V_{FS} = (k = \frac{1}{2}\Delta K)V_{REF}$

On the other hand, an actual half scale output V_{HS} of the combined D/C converter appears when only one of the two D/C converters, for example, DAC-1 is put in the full scale condition. The actual half scale output V_{HF} is expressed as follows:

$V_{HF} = K \bullet V_{REF}$

Accordingly, the linearity error $V_{LE(HS)}$ in the half scale is expressed:

$V_{LE(HS)} = V_{HS} = \frac{1}{2}V_{FS} = \frac{1}{2}\Delta K \bullet V_{REF}$

The ratio L.E. of $V_{LE(HS)}$ to the full scale is as follows:

$$L.E. = V_{LE(HS)} / V_{FS}$$

$$= \frac{1}{2}\Delta K / (2K - \Delta K)$$

$$\doteqdot \frac{1}{4} \cdot \frac{\Delta K}{K}$$

On the other hand, the full scale voltage V_{FS} in the combined D/A converter shown in Figure 4 is expressed as follows:

$V_{FS} = (2K - \Delta K)V_{REF}$

Namely, this is similar to that of the conventional accumulation method. Further, the magnitude of change V_{STEP} caused by the LBSs of the DAC-1 and DAC-2 is expressed:

$V_{STEP(1)} = K \bullet V_{REF} / 2\ell$

$V_{STEP(2)} = (K - \Delta K) \bullet V_{REF} / 2^{\ell}$

The linearity error due to the gain error will therefore appear at every two steps over the whole of the dynamic range. But, the magnitude of the error is compressed.

As ideal neutral point potential of the two steps can be expressed:

$$V_{STEP} / 2 = \left(k - \frac{\Delta K}{2}\right) V_{REF} / 2\ell$$

But, the actual neutral point potential is as follows:

$V_{STEPA} / 2 = (K - \Delta K)V_{REF} / 2^{\ell}$

Accordingly, the linearity error V_{LE} can be expressed:

$$V_{LE} = \frac{V_{STEP}}{2} - \frac{V_{STEPA}}{2}$$

$$= \frac{\Delta K}{2} \cdot V_{REF} / 2^{\ell}$$

The ratio L.E. can be expressed:

$$L.E. = \frac{V_{LE}}{V_{FS}} = \frac{2}{2K - \Delta K} \cdot \frac{\Delta K}{2} \cdot \frac{1}{2^{\ell}}$$

$$\fallingdotseq \frac{1}{4} \cdot \frac{1}{2^{\ell}} \cdot \frac{\Delta K}{K}$$

As seen from the above, the ratio L.E. of the combined D/A converter in accordance with the present invention is compressed to $1/2^{\ell}$ in comparison to the conventional accumulation method.

Referring to Figure 5, there is shown one embodiment of the A/D converter in accordance with the present invention. In Figure 4, elements similar to those shown in Figure 3 are given the same Reference Numerals, and explanation will be omitted. For simplification of drawing and explanation, the shown A/D converter is adapted to output a 6 bit digital signal. Namely, n = 6. Further, the shown converter is constructed on the condition of $\ell = 4$, $m = 2$ and $k = 2^2 = 4$. In the first embodiment shown in Figure 5, further, a voltage V_R is applied to the first reference potential terminal 46, and the second reference potential terminal 48 is grounded. In addition, a voltage $V_R/2$ is applied to the third reference potential terminal 40. Under these conditions, four local D/A converters 34A, 34B, 34C and 34D are provided, and the capacitances of the capacitors included in a capacitor array of each D/A converter are determined to fulfil the following relation:

$C_{10} = C_{11} = C_{20} = C_{21} = C_{30} = C_{31} = C_{40} = C_{41} = 1C$,
$C_{12} = C_{22} = C_{32} = C_{42} = 2C$,
$C_{13} = C_{23} = C_{33} = C_{43} = 4C$,
$C_{14} = C_{24} = C_{34} = C_{44} = 8C$.

Therefore, the capacitor 50 has a capacitance C_c of 64C.

Next, an A/D conversion operation will be explained. First, all the switches $S_{10} \sim S_{14}$, $S_{20} \sim S_{24}$, $S_{30} \sim S_{34}$ and $S_{40} \sim S_{44}$ are controlled to connect the analog signal input 30, and the switches 52 and 54 are closed. In this condition, an analog signal V_{in} applied to the input 30 is sampled in all the capacitor arrays of the D/A converters 34A to 34D in comparison to the third reference potential $V_R/2$.

Next, the switches 52 and 54 are turned off, and at the same time, the bit data D_1 to D_6 of the successive approximate register 42 is changed to such a condition that D_1 = "1" and $D_2 \sim D_6$ = "0". As a result, all the switches $S_{10} \sim S_{14}$, $S_{20} \sim S_{24}$, $S_{30} \sim S_{34}$, $S_{40} \sim S_{44}$ are separated from the analog signal input 30. In addition, since the bit data D_1 is brought to "1", all the switches S_{14}, S_{24}, S_{34} and S_{44} connected to the capacitors C_{14}, C_{24}, C_{34} and C_{44} of the capacitance 8C are connected to the first reference potential terminal 46 of the potential V_R. Since the other bit data D_2 to D_6 are kept at "0", the other switches $S_{10} \sim S_{13}$, $S_{20} \sim S_{23}$, $S_{30} \sim S_{33}$ and $S_{40} \sim S_{43}$ are connected to the second reference potential terminal 48 of the ground level. In this condition, comparison is made by the comparator 36. Namely, there has been performed a comparison step for the most significant bit (MSB) in the successive approximation system.

Now, assuming that the respective potentials of the inverted input and the non-inverted input of the comparator 36 are V_I and V_N, respectively, the following relation can be formed:

$$V_N = V_R/2$$

$$(\frac{V_R}{2} - V_{IN})\,64C = (V_I - V_R)\,32C + (V_I - 0)\,32C$$

$$V_I = V_R - V_{IN}$$

In case of $V_N > V_R/2$, the comparator 36 will output a logic signal of "1". To the contrary, if $V_{IN} < V_R/2$, the comparator 36 outputs a logic signal of "0". The logic output of the comparator 36 is applied to the successive approximation register 42, and as a result, the operation will enter the comparison step for the second significant bit (2SB). Specifically, with $V_{IN} > V_R/2$, the bit data D_1 and D_2 are put at "1" and the other bit data D_3 to D_6 are put at "0", with the result that the switches S_{13}, S_{14}, S_{24}, S_{34} and S_{44} are connected to the first reference potential V_R, and the other switches $S_{10} \sim S_{12}$, $S_{20} \sim S_{23}$, $S_{30} \sim S_{33}$ and $S_{40} \sim S_{43}$ are connected to the second reference potential of the ground level. In this condition, the following relation is established:

$$V_N = V_R/2$$

$$(\frac{V_R}{2} - V_{IN})\,64C = (V_I - V_R)\,(32C + 16C) + (V_I - 0)\,16C$$

$$V_I = \frac{5}{4}V_R - V_{IN}$$

As a result, if $V_{IN} > 3V_R/4$, the comparator 36 outputs a signal of "1". On the other hand, if $V_{IN} < 3V_R/4$, the comparator 36 generates a signal of "0". The output of the comparator 36 is applied to the successive approximation register 42.

The above operation will be repeated until the comparison for the least significant bit (LSB) is executed. The comparison result for the LSB is then inputted to the successive approximation register 42, and so, the content of the register is outputted through the output terminal as the result of the A/D conversion.

The following TABLE 2 and TABLE 3 indicate the correspondence between the bit data $D_1 \sim D_6$ and the position of the switches of all the D/A converters which can be taken in the course of the successive approximation operation. In these tables, "1" appearing in the switch position columns indicates that the switch is connected to the first reference potential, and "0" appearing in the switch position columns shows the switch is connected to the second reference potential.

TABLE 2

$D_1D_2D_3D_4D_5D_6$	$S_{14}S_{13}S_{12}S_{11}S_{10}$	$S_{24}S_{23}S_{22}S_{21}S_{20}$	$S_{34}S_{33}S_{32}S_{31}S_{30}$	$S_{44}S_{43}S_{42}S_{41}S_{40}$
BIT · DATA	D/A CONVERTER 34A	D/A CONVERTER 34B	D/A CONVERTER 34C	D/A CONVERTER 34D
0 1 1 1 1 1	1 2 2 2 2	1 2 2 2 2	1 2 2 2 2	2 1 1 1 2
0 1 1 1 1 0	1 2 2 2 2	1 2 2 2 2	2 1 1 1 2	2 1 1 1 2
0 1 1 1 0 1	1 2 2 2 2	2 1 1 1 2	2 1 1 1 2	2 1 1 1 2
0 1 1 1 0 0	2 1 1 1 2	2 1 1 1 2	2 1 1 1 2	2 1 1 1 2
0 1 1 0 1 1	2 1 1 1 2	2 1 1 1 2	2 1 1 1 2	2 1 1 2 2
0 1 1 0 1 0	2 1 1 1 2	2 1 1 1 2	2 1 1 2 2	2 1 1 2 2
0 1 1 0 0 1	2 1 1 1 2	2 1 1 2 2	2 1 1 2 2	2 1 1 2 2
0 1 1 0 0 0	2 1 1 2 2	2 1 1 2 2	2 1 1 2 2	2 1 1 2 2
0 1 0 1 1 1	2 1 1 2 2	2 1 1 2 2	2 1 1 2 2	2 1 2 1 2
0 1 0 1 1 0	2 1 1 2 2	2 1 1 2 2	2 1 2 1 2	2 1 2 1 2
0 1 0 1 0 1	2 1 1 2 2	2 1 2 1 2	2 1 2 1 2	2 1 2 1 2
0 1 0 1 0 0	2 1 2 1 2	2 1 2 1 2	2 1 2 1 2	2 1 2 1 2
0 1 0 0 1 1	2 1 2 1 2	2 1 2 1 2	2 1 2 1 2	2 1 2 2 2
0 1 0 0 1 0	2 1 2 1 2	2 1 2 1 2	2 1 2 2 2	2 1 2 2 2
0 1 0 0 0 1	2 1 2 1 2	2 1 2 2 2	2 1 2 2 2	2 1 2 2 2
0 1 0 0 0 0	2 1 2 2 2	2 1 2 2 2	2 1 2 2 2	2 1 2 2 2
0 0 1 1 1 1	2 1 2 2 2	2 1 2 2 2	2 1 2 2 2	2 2 1 1 2
0 0 1 1 1 0	2 1 2 2 2	2 1 2 2 2	2 2 1 1 2	2 2 1 1 2
0 0 1 1 0 1	2 1 2 2 2	2 2 1 1 2	2 2 1 1 2	2 2 1 1 2
0 0 1 1 0 0	2 2 1 1 2	2 2 1 1 2	2 2 1 1 2	2 2 1 1 2
0 0 1 0 1 1	2 2 1 1 2	2 2 1 1 2	2 2 1 1 2	2 2 1 2 2
0 0 1 0 1 0	2 2 1 1 2	2 2 1 1 2	2 2 1 2 2	2 2 1 2 2
0 0 1 0 0 1	2 2 1 1 2	2 2 1 2 2	2 2 1 2 2	2 2 1 2 2
0 0 1 0 0 0	2 2 1 2 2	2 2 1 2 2	2 2 1 2 2	2 2 1 2 2
0 0 0 1 1 1	2 2 1 2 2	2 2 1 2 2	2 2 1 2 2	2 2 2 1 2
0 0 0 1 1 0	2 2 1 2 2	2 2 1 2 2	2 2 2 1 2	2 2 2 1 2
0 0 0 1 0 1	2 2 1 2 2	2 2 2 1 2	2 2 2 1 2	2 2 2 1 2
0 0 0 1 0 0	2 2 2 1 2	2 2 2 1 2	2 2 2 1 2	2 2 2 1 2
0 0 0 0 1 1	2 2 2 1 2	2 2 2 1 2	2 2 2 1 2	2 2 2 2 2
0 0 0 0 1 0	2 2 2 1 2	2 2 2 1 2	2 2 2 2 2	2 2 2 2 2
0 0 0 0 0 1	2 2 2 1 2	2 2 2 2 2	2 2 2 2 2	2 2 2 2 2
0 0 0 0 0 0	2 2 2 2 2	2 2 2 2 2	2 2 2 2 2	2 2 2 2 2

TABLE 3

$D_1D_2D_3D_4D_5D_6$	$S_{14}S_{13}S_{12}S_{11}S_{10}$	$S_{24}S_{23}S_{22}S_{21}S_{20}$	$S_{34}S_{33}S_{32}S_{31}S_{30}$	$S_{44}S_{43}S_{42}S_{41}S_{40}$
111111	11111	11111	11111	11112
111110	11111	11111	11112	11112
111101	11111	11112	11112	11112
111100	11112	11112	11112	11112
111011	11112	11112	11112	11122
111010	11112	11112	11122	11122
111001	11112	11122	11122	11122
111000	11122	11122	11122	11122
110111	11122	11122	11122	11212
110110	11122	11122	11212	11212
110101	11122	11212	11212	11212
110100	11212	11212	11212	11212
110011	11212	11212	11212	11222
110010	11212	11212	11222	11222
110001	11212	11222	11222	11222
110000	11222	11222	11222	11222
101111	11222	11222	11222	12112
101110	11222	11222	12112	12112
101101	11222	12112	12112	12112
101100	12112	12112	12112	12112
101011	12112	12112	12112	12122
101010	12112	12112	12122	12122
101001	12112	12122	12122	12122
101000	12122	12122	12122	12122
100111	12122	12122	12122	12212
100110	12122	12122	12212	12212
100101	12122	12212	12212	12212
100100	12212	12212	12212	12212
100011	12212	12212	12212	12222
100010	12212	12212	12222	12222
100001	12212	12222	12222	12222
100000	12222	12222	12222	12222
BIT • DATA	D/A CONVERTER 34A	D/A CONVERTER 34B	D/A CONVERTER 34C	D/A CONVERTER 34D

Turning to Figure 6, there is shown a circuit of the control signal generator 44 which can control the switches S_{10} ~ S_{14}, S_{20} ~ S_{24}, S_{30} ~ S_{34} and S_{40} ~ S_{44} in accordance with the TABLE 2 and TABLE 3. The generator 44 has a 6 bit parallel input for receiving the bit data D_1 ~ D_6 of the successive approximation register 42. The generator 44 comprises a number of AND gates, OR gates and NOR gates connected as

shown to form a decoder which generates logic signals S_{10} ~ S_{44} for control of switches in accordance with the TABLE 2 and the TABLE 3. When the logic signals S_{10} ~ S_{44} are at "1", the switch is connected to the first reference potential. On the other hand, with logic signal of "0", the switch is connected to the second reference potential.

Referring to Figure 7, there is shown another embodiment of the 6 bit A/D converter in accordance with the present invention. In this figure, elements similar to those shown in Figure 5 are given the same Reference Numerals, and explanation will be omitted.

In this embodiment, each of the local D/A converters 34A to 34D has six charge redistribution and sample and hold capacitors C_{10} ~ C_{15}, C_{20} ~ C_{25}, C_{30} ~ C_{35} and C_{40} ~ C_{45} and six associated switches S_{10} ~ S_{15}, S_{20} ~ S_{25}, S_{30} ~ S_{35} and S_{40} ~ S_{45}. The capacitors of the respective capacitor arrays have capacitances fulfiling the following relation.

$C_{10} = C_{11} = C_{20} = C_{21} = C_{30} = C_{31} = C_{40} = C_{41} = 1C$,

$C_{12} = C_{22} = C_{32} = C_{42} = 2C$,

$C_{13} = C_{14} = C_{15} = C_{23} = C_{24} = C_{25} = C_{33} = C_{34} = C_{35} = C_{43} = C_{44} = C_{45} = 4C$,

Therefore, the capacitor 50 has a capacitance of 64C, similarly to the embodiment shown in Figure 5.

In the second embodiment shown in Figure 7, the capacitors incorporated in the local D/A converters has a capacitance of 1C at minimum and a capacitance of 4C at maximum. Therefore, in the case that the A/D converter is fabricated on an integrated circuit, the capacitors can be formed with a high relative precision in capacitance, and therefore, a high A/D conversion accuracy can be obtained.

The following TABLE 4 and TABLE 5 indicate the correspondence between the bit data D_1 ~ D_6 of the register 42 and the position of the switches S_{10} ~ S_{45} in the case of the second embodiment shown in Figure 7. "1" and "2" in the switch position columns have the same meanings as those in TABLE 2 and TABLE 3.

TABLE 4

$D_1D_2D_3D_4D_5D_6$	$S_{11}S_{12}S_{13}S_{14}S_{15}S_{16}$	$S_{21}S_{22}S_{23}S_{24}S_{25}S_{26}$	$S_{31}S_{32}S_{33}S_{34}S_{35}S_{36}$	$S_{41}S_{42}S_{43}S_{44}S_{45}S_{46}$
BIT · DATA	D/A CONVERTER 34A	D/A CONVERTER 34B	D/A CONVERTER 34C	D/A CONVERTER 34D
0 1 1 1 1 1	2 1 1 2 2 2	2 1 1 2 2 2	2 1 1 2 2 2	2 2 1 1 1 2
0 1 1 1 1 0	2 1 1 2 2 2	2 1 1 2 2 2	2 2 1 1 1 2	2 2 1 1 1 2
0 1 1 1 0 1	2 1 1 2 2 2	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 1 2
0 1 1 1 0 0	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 1 2
0 1 1 0 1 1	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 2 2
0 1 1 0 1 0	2 2 1 1 1 2	2 2 1 1 1 2	2 2 1 1 2 2	2 2 1 1 2 2
0 1 1 0 0 1	2 2 1 1 1 2	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 1 2 2
0 1 1 0 0 0	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 1 2 2
0 1 0 1 1 1	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 2 1 2
0 1 0 1 1 0	2 2 1 1 2 2	2 2 1 1 2 2	2 2 1 2 1 2	2 2 1 2 1 2
0 1 0 1 0 1	2 2 1 1 2 2	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 1 2
0 1 0 1 0 0	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 1 2
0 1 0 0 1 1	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 2 2
0 1 0 0 1 0	2 2 1 2 1 2	2 2 1 2 1 2	2 2 1 2 2 2	2 2 1 2 2 2
0 1 0 0 0 1	2 2 1 2 1 2	2 2 1 2 2 2	2 2 1 2 2 2	2 2 1 2 2 2
0 1 0 0 0 0	2 2 1 2 2 2	2 2 1 2 2 2	2 2 1 2 2 2	2 2 1 2 2 2
0 0 1 1 1 1	2 2 1 2 2 2	2 2 1 2 2 2	2 2 1 2 2 2	2 2 2 1 1 2
0 0 1 1 1 0	2 2 1 2 2 2	2 2 1 2 2 2	2 2 2 1 1 2	2 2 2 1 1 2
0 0 1 1 0 1	2 2 1 2 2 2	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 1 2
0 0 1 1 0 0	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 1 2
0 0 1 0 1 1	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 2 2
0 0 1 0 1 0	2 2 2 1 1 2	2 2 2 1 1 2	2 2 2 1 2 2	2 2 2 1 2 2
0 0 1 0 0 1	2 2 2 1 1 2	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 1 2 2
0 0 1 0 0 0	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 1 2 2
0 0 0 1 1 1	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 2 1 2
0 0 0 1 1 0	2 2 2 1 2 2	2 2 2 1 2 2	2 2 2 2 1 2	2 2 2 2 1 2
0 0 0 1 0 1	2 2 2 1 2 2	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 1 2
0 0 0 1 0 0	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 1 2
0 0 0 0 1 1	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 2 2
0 0 0 0 1 0	2 2 2 2 1 2	2 2 2 2 1 2	2 2 2 2 2 2	2 2 2 2 2 2
0 0 0 0 0 1	2 2 2 2 1 2	2 2 2 2 2 2	2 2 2 2 2 2	2 2 2 2 2 2
0 0 0 0 0 0	2 2 2 2 2 2	2 2 2 2 2 2	2 2 2 2 2 2	2 2 2 2 2 2

TABLE 5

111111	1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 2
111110	1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 2	1 1 1 1 1 2
111101	1 1 1 1 1 1	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 1 2
111100	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 1 2
111011	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 2 2
111010	1 1 1 1 1 2	1 1 1 1 1 2	1 1 1 1 2 2	1 1 1 1 2 2
111001	1 1 1 1 1 2	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 1 2 2
111000	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 1 2 2
110111	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 2 1 2
110110	1 1 1 1 2 2	1 1 1 1 2 2	1 1 1 2 1 2	1 1 1 2 1 2
110101	1 1 1 1 2 2	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 1 2
110100	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 1 2
110011	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 2 2
110010	1 1 1 2 1 2	1 1 1 2 1 2	1 1 1 2 2 2	1 1 1 2 2 2
110001	1 1 1 2 1 2	1 1 1 2 2 2	1 1 1 2 2 2	1 1 1 2 2 2
110000	1 1 1 2 2 2	1 1 1 2 2 2	1 1 1 2 2 2	1 1 1 2 2 2
101111	1 1 1 2 2 2	1 1 1 2 2 2	1 1 1 2 2 2	2 1 1 1 1 2
101110	1 1 1 2 2 2	1 1 1 2 2 2	2 1 1 1 1 2	2 1 1 1 1 2
101101	1 1 1 2 2 2	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 1 2
101100	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 1 2
101011	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 2 2
101010	2 1 1 1 1 2	2 1 1 1 1 2	2 1 1 1 2 2	2 1 1 1 2 2
101001	2 1 1 1 1 2	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 1 2 2
101000	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 1 2 2
100111	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 2 1 2
100110	2 1 1 1 2 2	2 1 1 1 2 2	2 1 1 2 1 2	2 1 1 2 1 2
100101	2 1 1 1 2 2	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 1 2
100100	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 1 2
100011	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 2 2
100010	2 1 1 2 1 2	2 1 1 2 1 2	2 1 1 2 2 2	2 1 1 2 2 2
100001	2 1 1 2 1 2	2 1 1 2 2 2	2 1 1 2 2 2	2 1 1 2 2 2
100000	2 1 1 2 2 2	2 1 1 2 2 2	2 1 1 2 2 2	2 1 1 2 2 2
$D_1D_2D_3D_4D_5D_6$	$S_{15}S_{14}S_{13}S_{12}S_{11}S_{10}$	$S_{25}S_{24}S_{23}S_{22}S_{21}S_{20}$	$S_{35}S_{34}S_{33}S_{32}S_{31}S_{30}$	$S_{45}S_{44}S_{43}S_{42}S_{41}S_{40}$
BIT • DATA	D/A CONVERTER 34A	D/A CONVERTER 34B	D/A CONVERTER 34C	D/A CONVERTER 34D

Figure 8 shows a circuit of the control signal generator 44 for controlling the switches S_{10} ~ S_{15}, S_{20} ~ S_{25}, S_{30} ~ S_{35} and S_{40} ~ S_{45} of the A/D converter shown in Figure 7 in accordance with TABLE 4 and TABLE 5. Namely, the shown generator includes a number of AND gates, OR gates and NOR gates connected as shown to constitute a decoder which responds to the bit data D_1 ~ D_6 of the register 42 so as to generate control signals for all the switchs S_{10} ~ S_{45} in accordance with TABLE 4 and TABLE 5.

As will be apparent from the above description of the embodiments with the reference to the drawings, a n-bit successive approximation A/D converter can be constructed by using 2^m ℓ-bit local D/A converters (where $\ell < n$, and $n = \ell + m$) in parallel so as to form a combined D/A converter, and by successively and alternatively incrementing the 2^M D/A converters so that the combined analog output is incremented. With the arrangement, the gain error of each D/A converter is uniformly distributed over the range from zero to the full scale. Therefore, a large gain error will not appear as a whole. In addition, the linearity error can be greatly improved.

Further, since there are used a plurality of D/A converter of the bit number smaller than a desired bit number, when the A/D converter is fabricated on an integrated circuit, it is possible to suppress an adverse effect of dispersion in characteristics of components formed on the integrated circuit.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. An analog-to-digital converter which includes a plurality of digital-to-analog converting circuits, a control circuit connected to the digital-to-analog converting circuits to control the condition of the respective digital-to-analog converting circuits, a comparator having a first input connected commonly to outputs of the digital-to-analog converting circuits and a second input connected to receive a reference voltage, and a successive approximation register connected to an output of the comparator and adapted to control the control circuit, characterized in that the control circuit is adapted to generate control signals to the respective digital-to-analog converting circuits in one-to-one relation so that the output potentials of the digital-to-analog converting circuits are successively incremented one after one by a potential corresponding to one bit.

2. A converter as claimed in Claim 1 wherein each of the digital-to-analog converting circuit includes a charge redistribution binary weighted capacitor array.

3. A converter as claimed in Claim 2 wherein each capacitor array is composed of a plurality of sample and hold capacitors.

4. A converter as claimed in Claim 2 wherein the second input of the comparator is connected to one terminal of a capacitor means whose other terminal is connected to the reference voltage, the capacitor means having a capacitance equal to the total capacitance of all the capacitors included in all of the digital-to-analog converting circuits.

5. An n-bit analog-to-digital converter which includes 2^m ℓ-bit of digital-to-analog converting circuits (where $\ell < n$ and $n = m + \ell$), a control circuit connected to the digital-to-analog converting circuits to control the condition of the respective digital-to-analog converting circuits, a comparator having a first input connected commonly to outputs of the digital-to-analog converting circuits and a second input connected to receive a reference voltage, and a successive approximation register connected to an output of the comparator and adapted to control the control circuit, characterized in that the control circuit is adapted to generate control signals to the respective digital-to-analog converting circuits in one-to-one relation so that the output potentials of the digital-to-analog converting circuits are successively incremented one after one by a potential corresponding to one bit.

6. A converter as claimed in Claim 5 wherein each of the digital-to-analog converting circuit includes a charge redistribution binary weighted capacitor array.

7. A converter as claimed in Claim 6 wherein each capacitor array is composed of at least (ℓ + 1) sample and hold capacitors.

8. A converter as claimed in Claim 6 wherein each capacitor array is composed of (ℓ + 2) sample and hold capacitors.

9. A converter as claimed in Claim 6 wherein the second input of the comparator is connected to one terminal of a capacitor means whose other terminal is connected to the reference voltage, the capacitor means having a capacitance equal to the total capacitance of all the capacitors included in all of the digital-to-analog converting circuits.

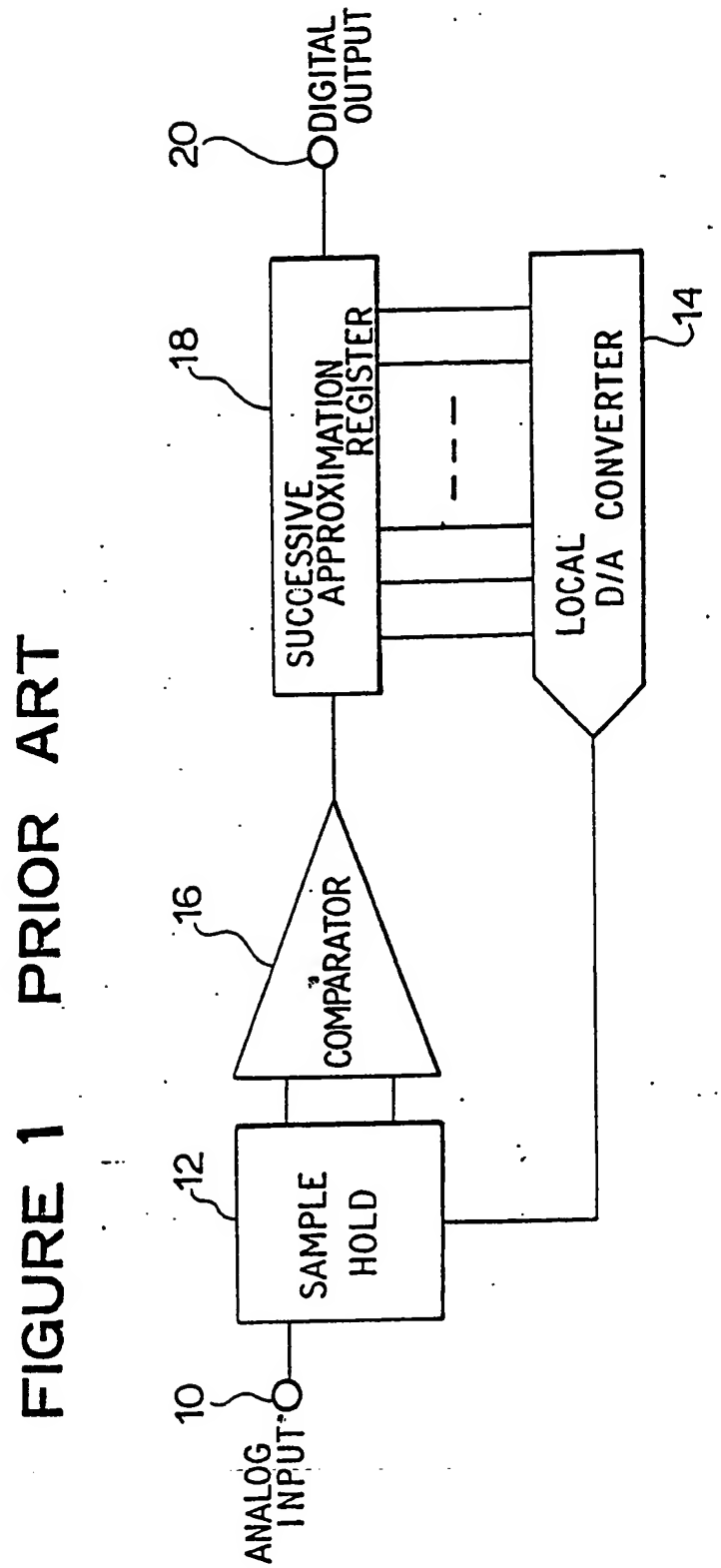
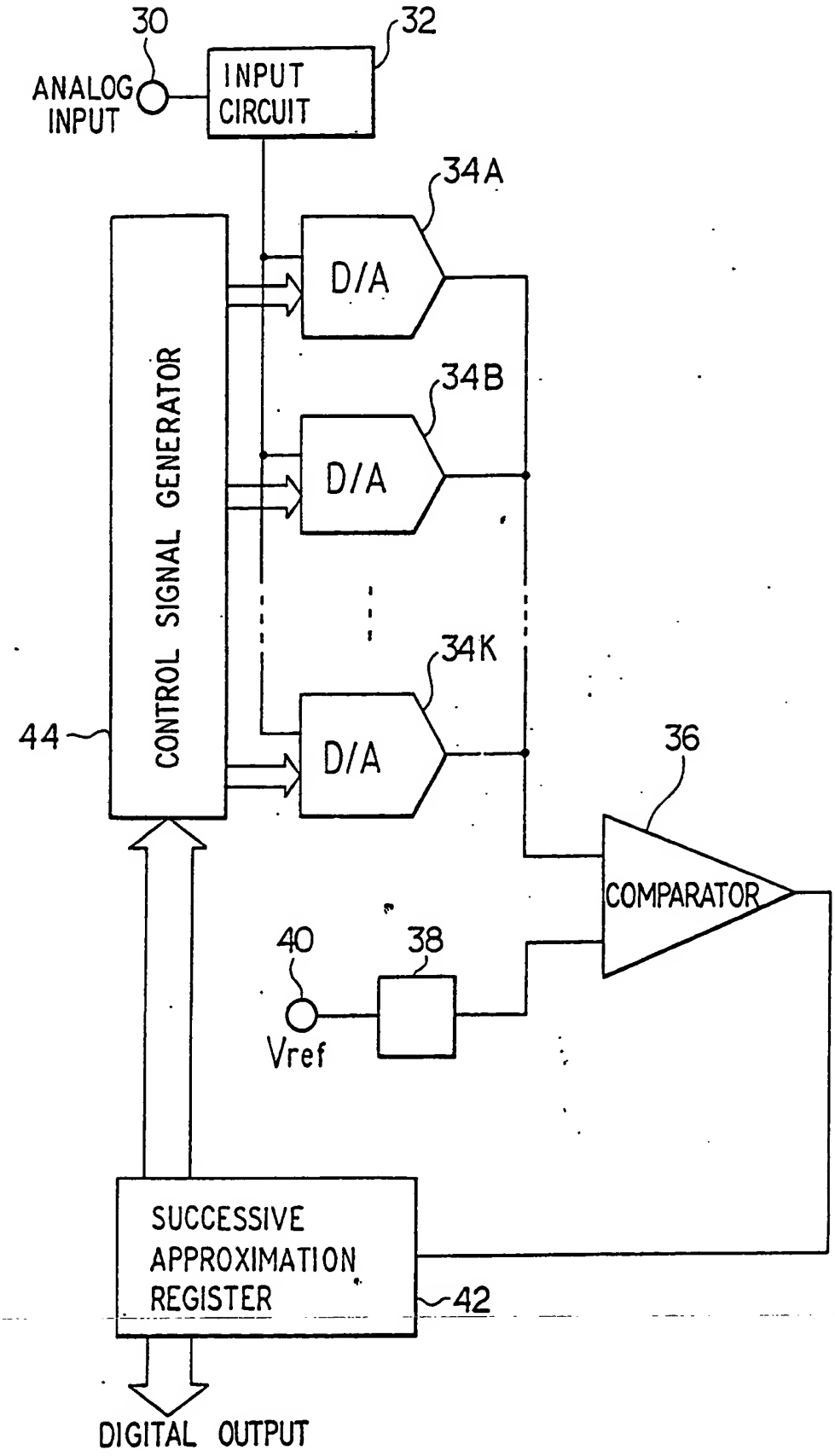


FIGURE 1 PRIOR ART

FIGURE 2


30
32
ANALOG INPUT
INPUT CIRCUIT
34A
D/A
34B
D/A
34K
D/A
44
CONTROL SIGNAL GENERATOR
36
COMPARATOR
40
38
Vref
SUCCESSIVE APPROXIMATION REGISTER
42
DIGITAL OUTPUT

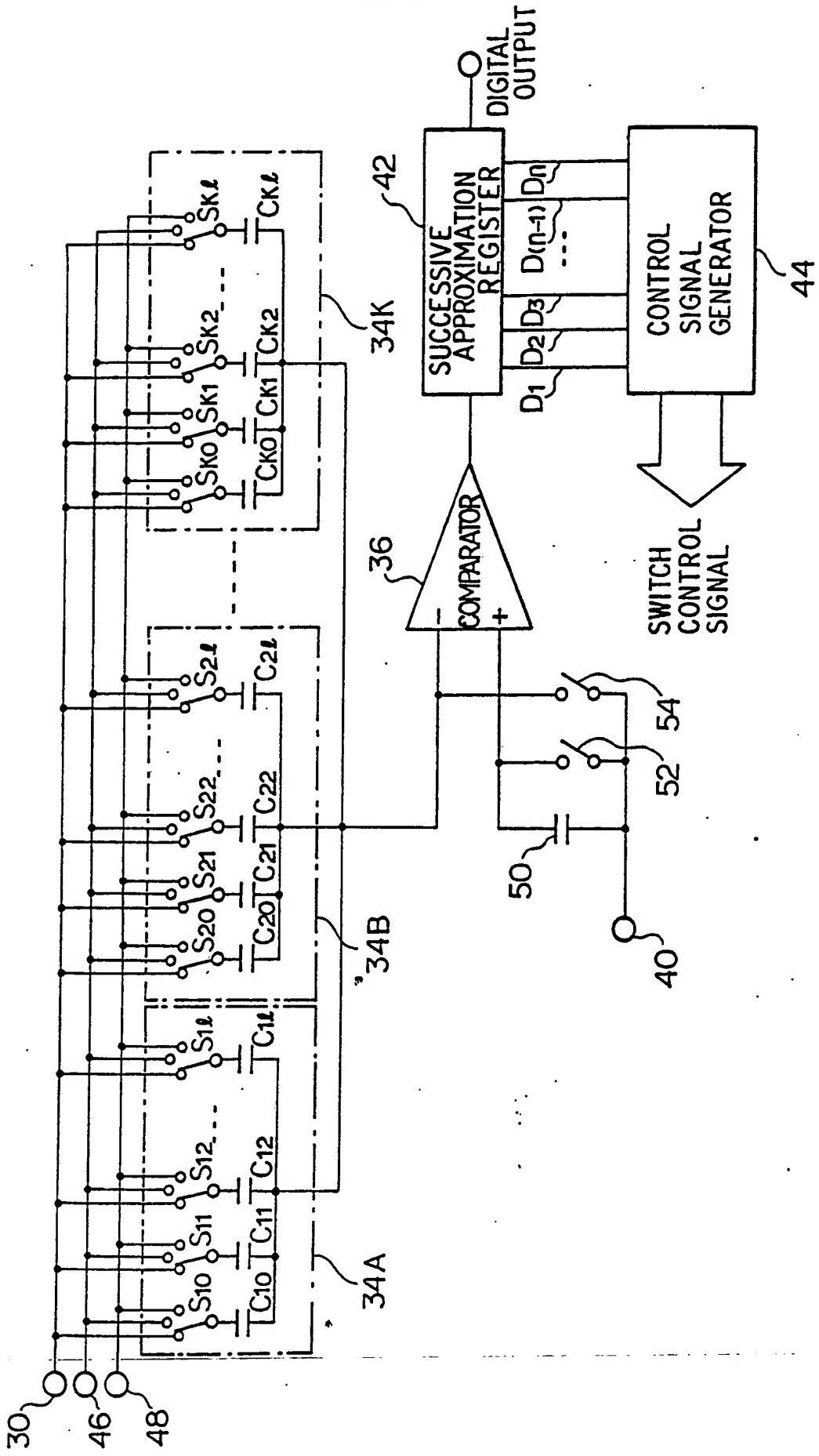

DIGITAL OUTPUT
SUCCESSIVE APPROXIMATION REGISTER
42
CONTROL SIGNAL GENERATOR
44
Dn
D(n-1)
D3
D2
D1
COMPARATOR
36
SWITCH CONTROL SIGNAL
34K
34B
34A
30
46
48
40
50
52
54
SK1
CK1
SK2
CK2
SK1
CK1
SK0
CK0
S21
C21
S22
C22
S21
C21
S20
C20
S11
C11
S12
C12
S11
C11
S10
C10

FIGURE 3

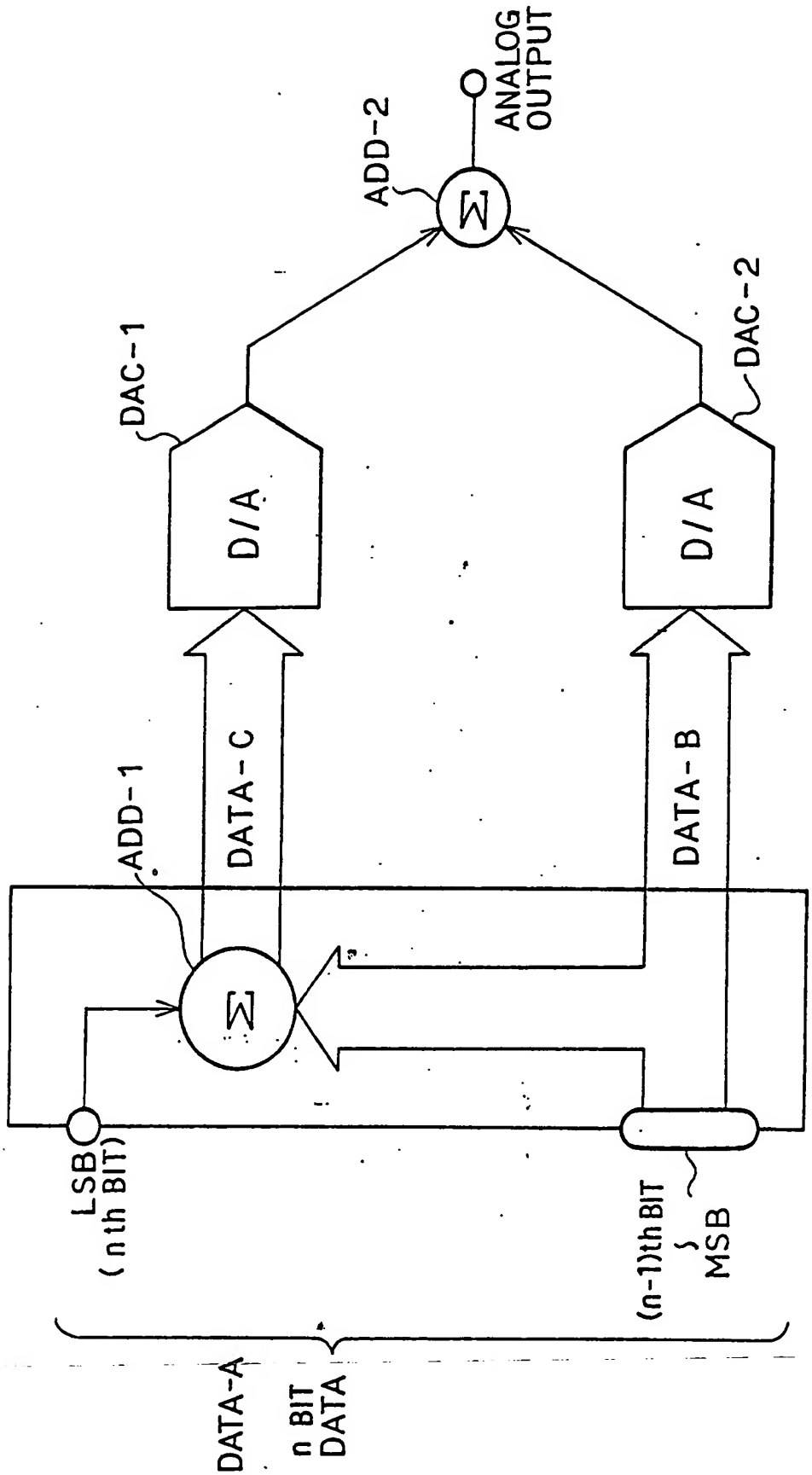

ANALOG OUTPUT
ADD-2
Σ
DAC-1
DAC-2
D/A
D/A
DATA-C
DATA-B
ADD-1
Σ
LSB (nth BIT)
(n-1)th BIT
MSB
DATA-A
n BIT DATA

FIGURE 4

FIGURE 5

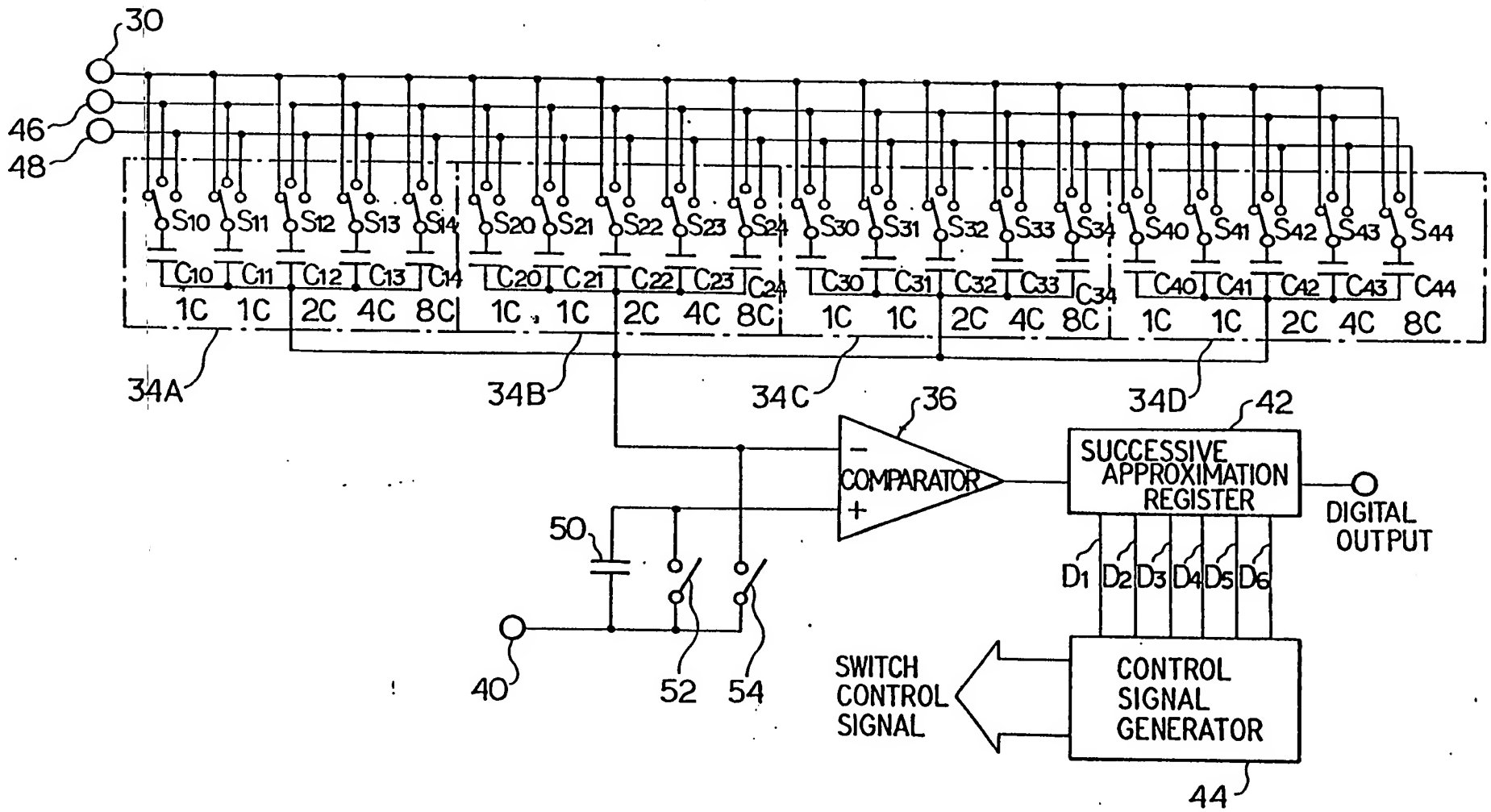

30
46
48
S10 S11 S12 S13 S14 S20 S21 S22 S23 S24 S30 S31 S32 S33 S34 S40 S41 S42 S43 S44
C10 C11 C12 C13 C14 C20 C21 C22 C23 C24 C30 C31 C32 C33 C34 C40 C41 C42 C43 C44
1C 1C 2C 4C 8C 1C 1C 2C 4C 8C 1C 1C 2C 4C 8C 1C 1C 2C 4C 8C
34A
34B
34C
34D
36
COMPARATOR
42
SUCCESSIVE APPROXIMATION REGISTER
DIGITAL OUTPUT
D1 D2 D3 D4 D5 D6
50
40
52
54
SWITCH CONTROL SIGNAL
CONTROL SIGNAL GENERATOR
44

FIGURE 6

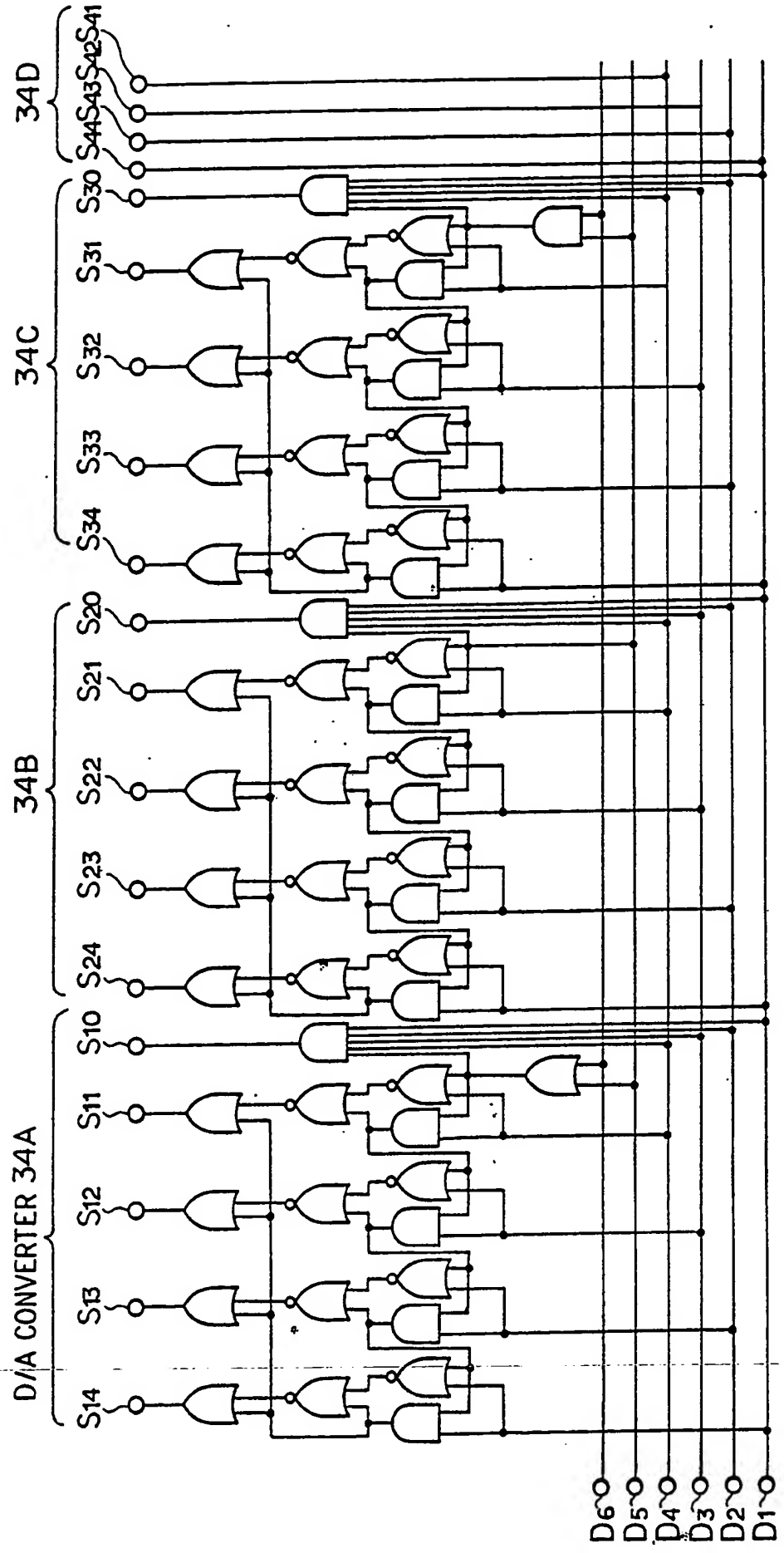

D/A CONVERTER 34A
34B
34C
34D
S14
S13
S12
S11
S10
S24
S23
S22
S21
S20
S34
S33
S32
S31
S30
S44
S43
S42
S41
D6
D5
D4
D3
D2
D1

FIGURE 7

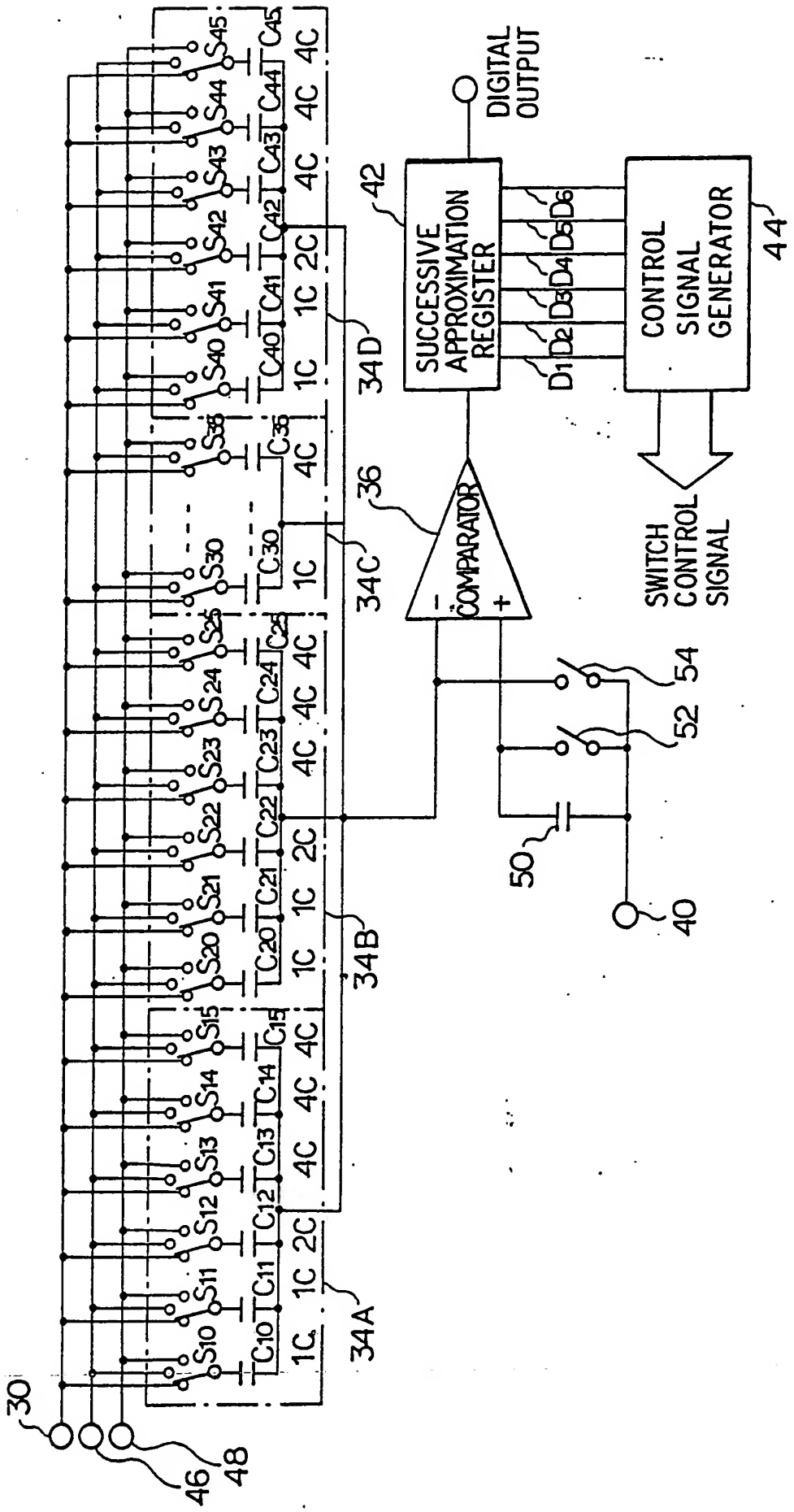
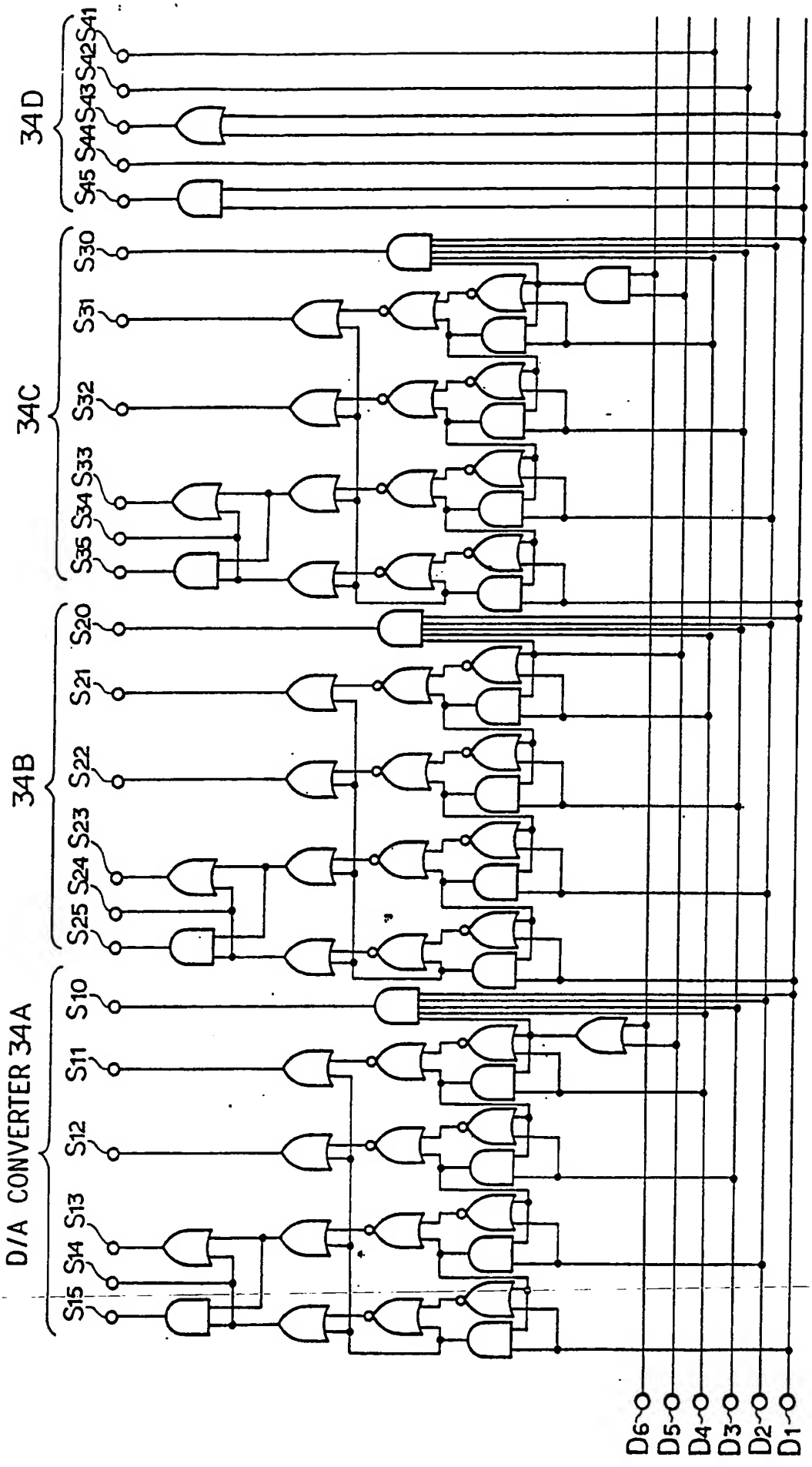

30
46
48
34A
34B
34C
34D
1C
2C
4C
S10
S11
S12
S13
S14
S15
S20
S21
S22
S23
S24
S25
S30
S33
S40
S41
S42
S43
S44
S45
C10
C11
C12
C13
C14
C15
C20
C21
C22
C23
C24
C25
C30
C35
C40
C41
C42
C43
C44
C45
36
COMPARATOR
42
SUCCESSIVE APPROXIMATION REGISTER
DIGITAL OUTPUT
D1
D2
D3
D4
D5
D6
44
CONTROL SIGNAL GENERATOR
SWITCH CONTROL SIGNAL
50
52
54
40

FIGURE 8


D/A CONVERTER 34A
34B
34C
34D
S10
S11
S12
S13
S14
S15
S20
S21
S22
S23
S24
S25
S30
S31
S32
S33
S34
S35
S41
S42
S43
S44
S45
D6
D5
D4
D3
D2
D1